UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,011,992 B2
APPLICATION NO. : 10/677278
DATED : March 14, 2006
INVENTOR(S) : Ki Yong Lee

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, Item (57), Abstract, replace the Abstract in its entirety with the Abstract below.

--A method of fabricating a TFT using dual or multiple gates, and a TFT having superior characteristics and uniformity by providing a method of fabricating a TFT using dual or multiple gates by calculating the probability including Nmax, the maximum number of crystal grain boundaries in active channel regions according to the length of the active channels, and adjusting a gap between the active channels capable of synchronizing the number of the crystal grain boundaries in each active channel region of the TFT using the dual or multiple gates in the case where Gs, the size of crystal grains of polycrystalline silicon forming a TFT substrate, θ angle in which "primary" crystal grain boundaries are inclined at a direction perpendicular to an active channel direction of the gates, the width of the active channels and the length of the active channels are determined.--

Column 12, line 4, change "claim 9" to --claim 8--.

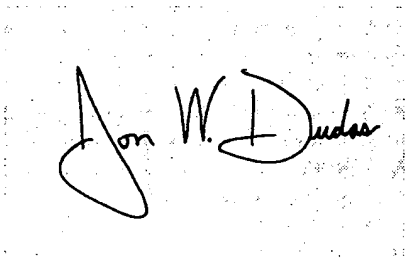
Column 12, line 7, insert --where Gs is the size of crystal grains, θ is an angle in which fatal crystal grain boundaries ("primary" crystal grain boundaries) are inclined at a direction perpendicular to an active channel direction, and L is the length of each active channel of each dual or multiple gates-- after "$S=mGs \cdot \sec\theta-L$".

Column 12, line 10, change "claim 8" to --claim 9--.

Column 12, line 20, change "claim 12" to --claim 10--.

Signed and Sealed this

Fourteenth Day of November, 2006



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